BROCHURE

Innovation for the next generation

V93000 HSIO High-Speed Solution

32 bidirectional differential Lane Count | BERT and DSO, Source/Measure up to 112 Gbps | NRZ and PAM4 | AWG with 96Gsa/s Fs | SmarTest API's | V93000 production ready| Loadboard accessories

Summary

Advantest and MultiLane offer a single platform solution which leverages the best capabilities and qualities of both companies. MultiLane high-speed BERT, scope DSO, and arbitrary waveform generator AWG high-speed instruments are fully integrated into Advantest's V93000 ATE tester, expanding digital and analog semiconductor IC characterization, validation and production testing capabilities. The BERT/DSO/AWG instruments provide testing capabilities of 32 differential lanes at up to 112 Gbps (PAM4) and 35 GHz bandwidth. V93000 Smartest software and hard docking solutions are already deployed worldwide, with proven reliable results in production environments.

This unique V93000 turnkey solution enables testing of packaged silicon as well as wafer probe, including at-speed testing of SerDes, transceivers, amplifiers, ASICs with high-speed I/O, and other active and passive high-speed devices. Testing is accomplished at the PHY level for Ethernet, USB 3/4, PCIe 5/6 and other high-speed serial I/O port types.

V93000 HSIO System Overview

The BERTs, DSOs, and AWGs are located directly under the load board, in the cavity of the test head extender called the Twinning Frame. Due to this proximity to the load board, the signal path from MultiLane instruments to the DUT is extremely short. This significantly enhances signal integrity and test accuracy.

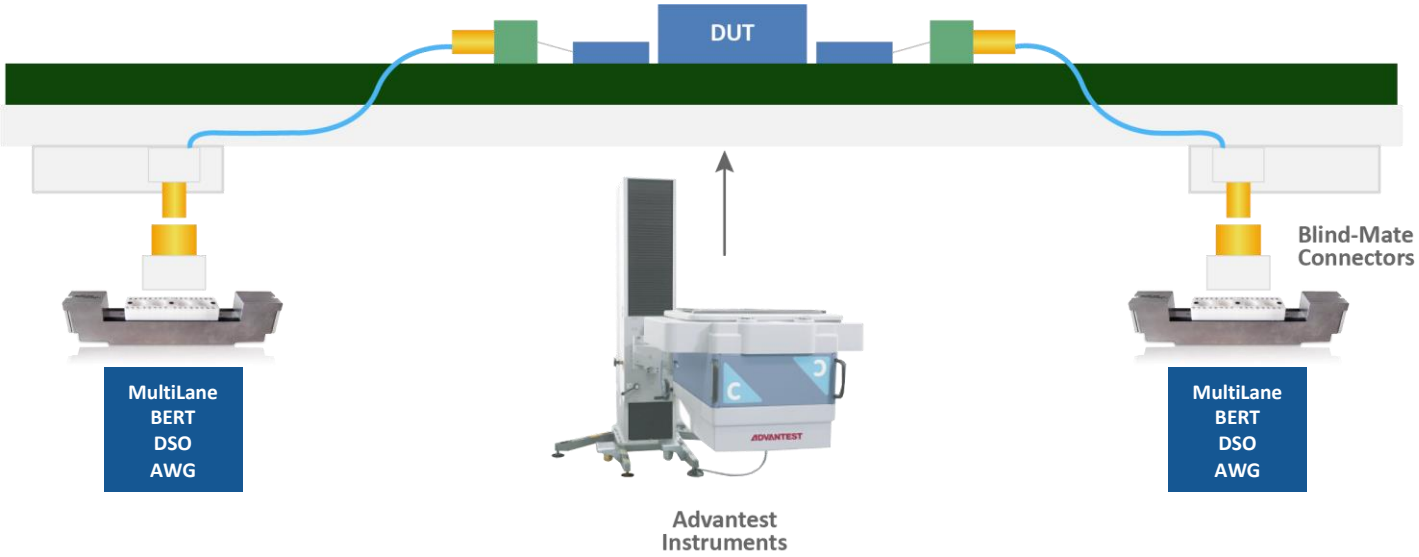

Figure 1: Overview of the V93000 HSIO System

Figure 2: Twinning Frame with MultiLane BERTs, DSOs, and AWGs inside.

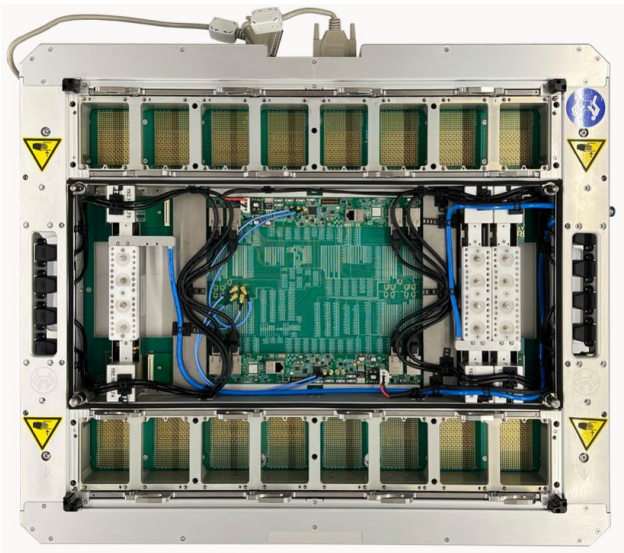

Figure 3: 3 of 4 HSIO MultiLane cassettes mounted inside a twinning frame.

Key Features and Benefits

Key Features

- 32 synchronized lane testing
- Arbitrary and PRBS NRZ & PAM4 signals
- Blindmate RF cable connection
- V93000 Smartest Software API's
- Multisite ready software
- Direct Docking
- At-Speed Wafer sort testing
- At-Speed Package testing
- Easy movement of capabilities between bench and AT
- A complete set of APIs and multiple SmarTest sample code to speed up integration

Key Benefits

- High-speed interface testing
- Complementary testing capabilities to the V93000 test platform
- BERTs and SCOPEs compensate for cable and DUT board traces
- SmarTest tools help speed test program development and multisite deployment
- Advantest docking allows quick and reliable interfacing to a wide variety of device handlers and wafer probers

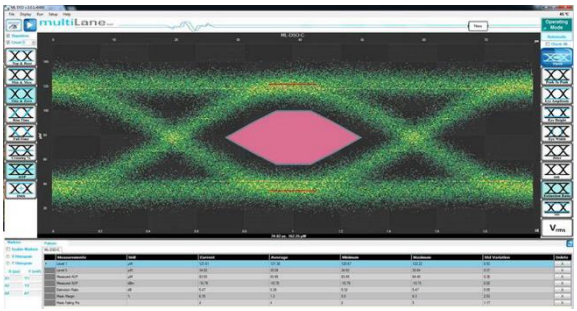

Figure 4: NRZ Eye Measurements

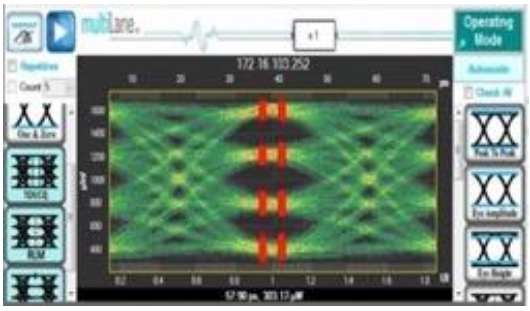

Figure 6: PAM4 Eye Measurements

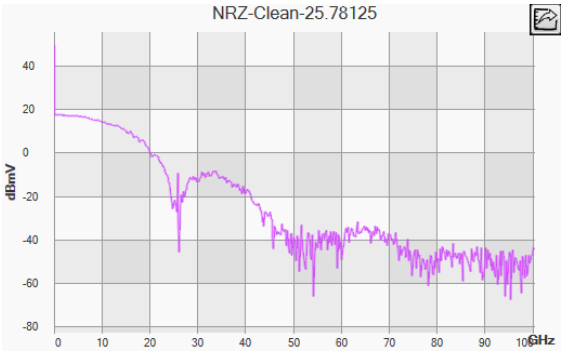

Figure 5: Measuring Total Harmonic Distortion

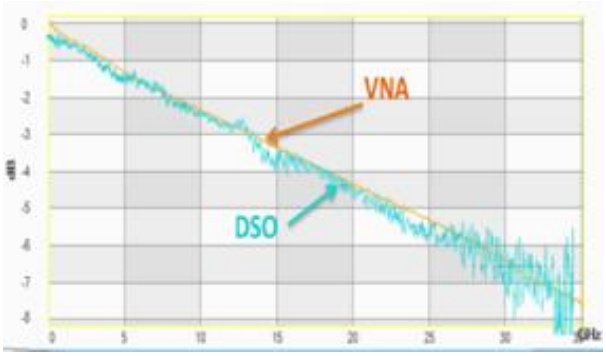

Figure 7: Correlated S21 measured - VNA and DSO

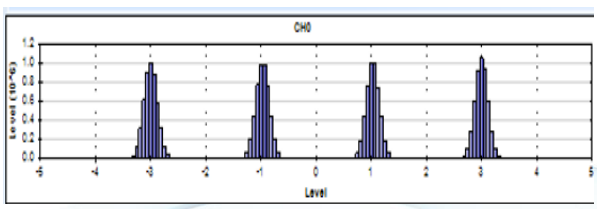

Figure 8: BERT PAM4 eye histogram

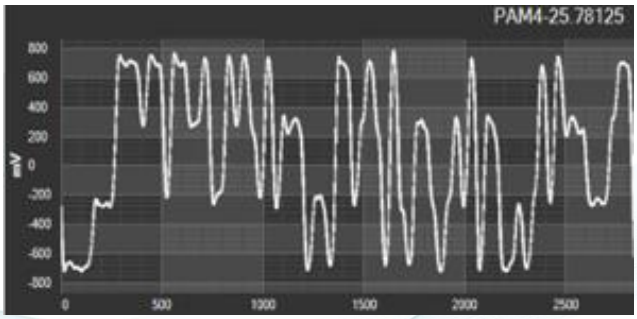

Figure 9: PAM4 signaling measured on DSO

multiLane

Instruments Specs

4-Ch 35 GHz Electrical DSO (AT4025)

DSO Features

- 35 GHz input bandwidth
- Fast sampling and multi-threaded DSP using optimized hardware and Smartest software.
- Extensive library of built-in DSP filters such as Bessel-Thomson, CTLE, DFE, FFE, de-embedding and component emulation
- De-embedding tools to compensate for insertion losses that are always present in high-speed signaling.
- Built-in standard masks library

4-Lane BERT 56 GBd PAM4/NRZ (AT4039E)
4-Lane BERT 28 GBd PAM4/NRZ (AT4039D)

PPG Features

- E-version
  - Up to 800 mVppd voltage swing
  - High-speed reference ≤7 GHz clock
- D-version
  - Up to 1500 mVppd voltage swing
  - High-speed reference ≤3 GHz clock
- PRBS 7, 9, 11, 13, 15, 16, 23, 31, 58
- PRBS 13Q, SSPRQ
- PRBS 31Q (E-version)
- PRBS patterns are generated algorithmically
- Real FEC and Gray coding, Polarity inversion
- Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed

Error Detection Features

- FFE Equalizers with reflection cancellation and DFE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS7, 9, 13, 15, 23 & 31 error checker
- Automatic PRBS detection
- Clock-data recover
- BER counters

4-Lane, 64GBaud AWG PAM4/NRZ (AT4080)

Key Features

- AWG mode: 96 Gsa/s sampling clock, 32K mem
- PRBS mode: 1-64 GBd selectable Baud Rate
- User defined modulation
- NRZ/PAM4 modulation
- Independent 7-tap FFE on each transmitter
- Generate coherent signals for QAM modulation
- Independent control of inner eye levels
- Tune the bit rate in very fine steps

8-Lane 1 – 28 GBd PAM4/NRZ (AT4079B)

Key Features

- Low-cost alternative to higher-speed and higher-swing 4-lane AT4039x BERTs
- Instrument-grade BERT optimized for high-speed data analysis of 100G/200G/400G transceivers
- Ability to tune the bit rate in very fine steps to facilitate finding the locking margin
- FEC support
- Supports PRBS13Q/15Q/31Q and user-defined patterns
- API library, sample code and Python wrapper Gray-coding, polarity inversion

SmarTest Software

V93000 Control

- Advantest Smartest 7.x and 8.x software API's
- Advantest Multisite software methodology
- Full use of all Advantest Smartest software features such as debugging and datalogging
- High throughput multithreaded DSP routines

Windows based control

- Alternative laptop Ethernet control path into MultiLane instruments using Multilane GUI window software

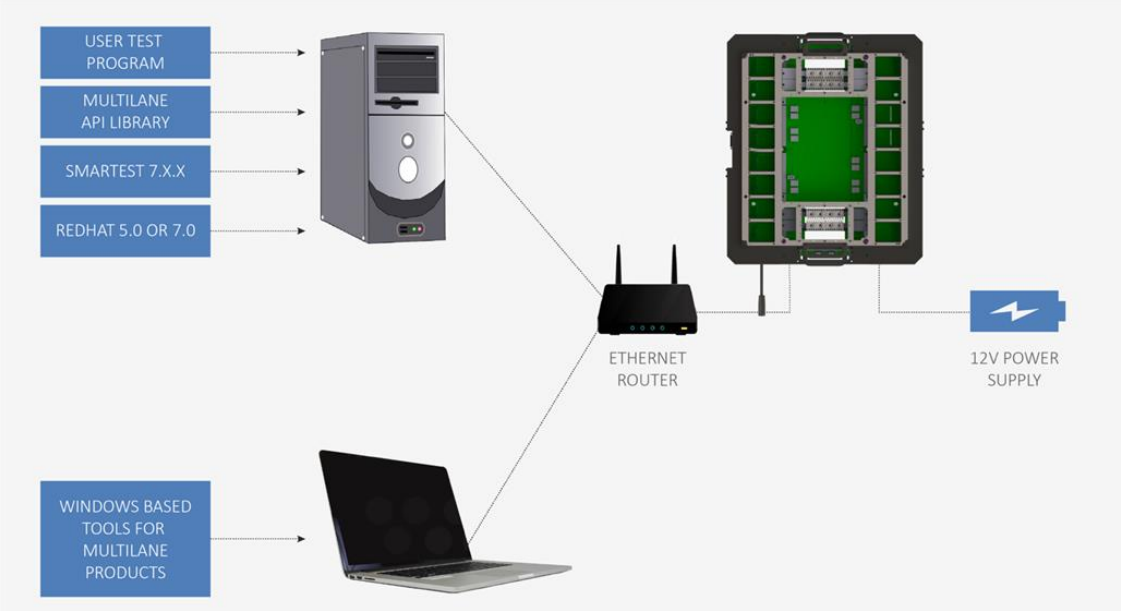

Figure 10: SmarTest Integration Model

Ordering Information

Details	Product Number
4-channel 50 GHz Bandwidth Digital Sampling Oscilloscope. ½ cassette	**AT4025**
4-lane 56 Gbps (28 GBaud PAM4/NRZ) BERT. ½-cassette	**AT4039D**
4-lane 112 Gbps (56 GBaud PAM4/NRZ) BERT. ½-cassette	**AT4039E**
8-Lane 60 Gbps (30 GBd PAM4/NRZ) BERT. 1-cassette	**AT4079B**
4-Lane, 64GBaud AWG & BERT PAM4/NRZ	**AT4080**
Twinning Frame infrastructure	**Contact MultiLane**
Package Test and Wafer Probe Test Loadboard Accessories	**Contact MultiLane**
Specialized high-speed cable assemblies	**Contact MultiLane**
ATE-related application services	**Contact MultiLane**

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